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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,200	01/27/2004	Joseph P. Miller	200313849-1	3318

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,200	MILLER, JOSEPH P.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. §.119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-16,19-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsushige (US Publication Number 20030101020A1). As per claim 1, Matsushige discloses adjusting a reference voltage signal from a first level to a second level in response to an output from the controller in the computer, the first level being a level of the reference voltage signal during normal operation of the computer; testing operation of a receiver in the computer with the reference voltage signal set at the second level, an input of the receiver being connected to the reference voltage signal; and adjusting the reference voltage signal back from the second level to the first level to enable normal operation of the computer on page 5, paragraph 0085; on page 7, paragraphs 0127-129; on page 8, paragraph 0139..

3. As per claim 2, Matsushige discloses wherein testing the operation of the receiver comprises testing operation of the receiver that receives a single-ended signal on page 5, paragraph 085; on page 7, paragraphs 0127-0129.

4. As per claim 3, Matsushige discloses wherein testing the operation of the receiver comprises testing operation of a differential receiver on page 5, paragraph 085.

5. As per claim 4, Matsushige discloses further comprising testing operation of a second receiver, the second receiver being connected to the reference voltage signal on page 5, paragraph 0085; page 7, paragraphs 0127-0129,0137.

6. As per claim 5, Matsushige discloses wherein the computer comprises a bus having transmission lines for carrying plural signals, the method further comprising transmitting the plural signals over the transmission lines to the receivers on page 5, paragraph 0085,0086.

7. As per claim 6, Matsushige discloses wherein transmitting the plural signals is performed by transmitters in a bus device connected to the bus on page 7, paragraphs 0127-0129.

8. As per claim 7, Matsushige discloses further comprising controlling the output of the controller by a software routine on page 7, paragraphs 0127-0129.

9. As per claim 8, Matsushige discloses wherein controlling the output of the controller comprises controlling a general purpose input/output (GPIO) port of the controller on page 7, paragraphs 0127-0129. The buffer is the memory containing configuration information file.

10. As per claim 9, Matsushige discloses further comprising indicating a margin of the reference voltage signal as poor in response to the testing producing an error on page 5, paragraph 0085; on page 7, paragraphs 0127-0129.

11. As per claim 10, Matsushige discloses wherein adjusting the reference voltage signal comprises a test circuit adjusting the reference voltage signal, the test circuit responsive to the output of the controller on page 5, paragraph 0085; on page 7, paragraphs 0127-0129.

12. As per claim 11, Matsushige discloses a processor; test software executable on the processor; a circuit to generate a reference voltage signal; a receiver having an input connected to the reference voltage signal; and the circuit responsive to the test software to adjust a voltage level of the reference voltage signal from a first voltage level to a second voltage level, the test software to perform a diagnostic test with the reference voltage signal at the second voltage level to test operation of the receiver on page 5, paragraph 0085; on page 7, paragraphs 0127-0129.

13. As per claim 12, Matsushige discloses further comprising a second receiver having an input connected to the reference voltage signal, the diagnostic test to also test operation of the second receiver on page 7, paragraphs 0127-0132,0137.

14. As per claim 13, Matsushige discloses wherein the receivers are differential receivers each having a second input connected to a respective single-ended signal on page 5, paragraph 0085.

15. As per claim 14, Matsushige discloses further comprising a bus, wherein the bus comprises transmission lines to carry the single-ended signals on page 5, paragraph 0085.

16. As per claim 15, Matsushige discloses further comprising: a transmitter to generate a single-ended signal, wherein the receiver has a second input connected to the single-ended signal on page 5, paragraph 0085; page 7, paragraphs 0127-0129.

17. As per claim 16, Matsushige discloses further comprising a general purpose input/output (GPIO) buffer responsive to commands from the test software to control the voltage level of the reference voltage signal produced by the circuit on page 7, paragraphs 0127-0129. The buffer is the memory containing configuration information file.

18. As per claim 19, Matsushige discloses wherein the circuit comprises a digital-to-analog converter responsive to the test software on page 3, paragraph 0058.

19. As per claim 20, Matsushige discloses a processor; software executable on the processor; means for generating a reference voltage signal; and receiving means having an input connected to the reference voltage signal; wherein the generating means is responsive to the software to adjust a voltage level of the reference voltage signal from a first voltage level to a second voltage level, and the software to perform a diagnostic test with the reference voltage signal at the second voltage level to test operation of the receiving means on page 5, paragraph 0085; on page 7, paragraphs 0127-0129.

20. As per claim 21, Matsushige discloses a transmitter to transmit a single-ended signal; a circuit to generate a reference voltage signal; a receiver having a first input connected to the single-ended signal, and a second input connected to the reference voltage signal; and a controller to control the circuit to vary a voltage level of the

reference voltage signal, wherein the controller is adapted to perform a diagnostic test after varying the voltage level of the reference voltage signal on page 5, paragraph 0085; on page 7, paragraphs 0127-0129. The transmitter is the microprocessor. The receiver is the drive.

21. As per claim 22, Matsushige discloses wherein the controller is adapted to control the circuit to vary the voltage level of the reference voltage signal from a first voltage level to a second voltage level, the first voltage level corresponding to a voltage level of the reference voltage signal for normal operation, the controller adapted to perform the diagnostic test with the reference voltage signal set at the second voltage level on page 5, paragraph 0085; on page 7, paragraphs 0127-0129.

22. As per claim 23, Matsushige discloses wherein the receiver comprises a differential receiver on page 5; paragraph 0085.

23. As per claim 24, Matsushige discloses wherein the controller comprises software on page 7, paragraphs 0127-0129.

24. As per claim 25, Matsushige discloses send commands to a circuit to cause a voltage level of a reference voltage signal to be adjusted from a first level to a second level, the first level corresponding to a voltage level of the reference voltage signal during normal operation; and perform a diagnostic test of a receiver having an input connected to the reference voltage signal with the reference voltage signal at the second level on page 5, paragraph 0085; on page 7, paragraphs 0127-0129.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige in view of Wikipedia (voltage divider rule). As per claim 17, Matsushige fails to explicitly state wherein the circuit comprises a voltage divider to produce the reference voltage signal, the circuit further comprising a resistor connected to the voltage divider to adjust the voltage level of the reference voltage signal from the first voltage level to the second voltage level.

Wikipedia discloses this limitation on page 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the circuit comprises a voltage divider to produce the reference voltage signal, the circuit further comprising a resistor connected to the voltage divider to adjust the voltage level of the reference voltage signal from the first voltage level to the second voltage level. A person of ordinary skill in the art would have been motivated to have the circuit comprises a voltage divider to produce the reference voltage signal, the circuit further comprising a resistor connected to the voltage divider to adjust the voltage level of the reference voltage signal from the first voltage level to the second voltage level because with in a voltage divider circuit reference voltage can be altered to a different voltage.

27. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige in view of Wikipedia (potentiometer). As per claim 18, Matsushige fails to explicitly state wherein the circuit comprises an electronically adjustable potentiometer responsive to the test software.

Wikipedia discloses this limitation on page 1.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the circuit comprises an electronically adjustable potentiometer responsive to the test software. A person of ordinary skill in the art would have been motivated to have the circuit comprises an electronically adjustable potentiometer responsive to the test software because the potentiometer has an adjustable resistance.

Claim Rejections - 35 USC § 101

28. 35 U.S.C. 101 reads as follows:

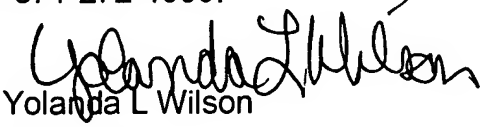
> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

29. Claim 25 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The storage medium disclosed in claim 25 is directed to non-statutory subject matter, a carrier wave disclosed in paragraph 0058.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Yolanda L Wilson
Examiner
Art Unit 2113